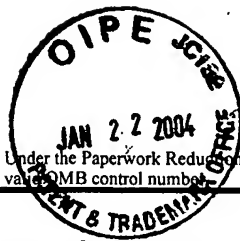
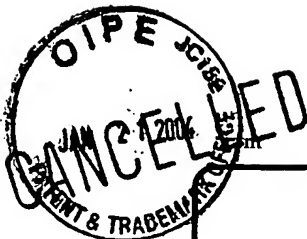


6 01.27.04 2631



Modified 02-03

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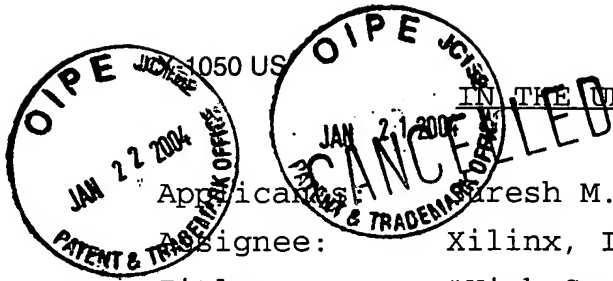
TRANSMITTAL FORM (to be used for all correspondence after initial filing)		Application / Conf. No.	10/090,250 / 4098
		Filing Date	March 01, 2002
		First Named Inventor	Suresh M. Menon
		Examiner Name	Unknown
		Art Unit	2631
Mail Stop:		Patent No.	
Express Mail Receipt No.		Attorney Docket Number	X-1050 US
Total Number of Pages in This Submission			

ENCLOSURES (check all that apply)		
<input type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Assignment Papers (with Recordation Cover Sheet)	<input type="checkbox"/> After Allowance Communication to
<input type="checkbox"/> Amendment / Reply	<input type="checkbox"/> Declaration / Oath	<input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences
<input type="checkbox"/> Preliminary Amendment	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
<input type="checkbox"/> After Final	<input type="checkbox"/> Licensing-related Papers	<input type="checkbox"/> Status Letter
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<input type="checkbox"/> Extension of Time Request	<input type="checkbox"/> To Convert a Provisional Application	<input checked="" type="checkbox"/> Other Enclosure(s) (please identify below):
<input type="checkbox"/> Change Status to LARGE ENTITY	<input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address	One Copy each of the One Hundred Seven (107) references cited
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<input type="checkbox"/> Certified Copy of Priority Document(s)		
<input type="checkbox"/> Response to Missing Parts/Incomplete Application	Remarks	
<input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT		
Firm or Customer Number	24309	Reg. Number 51,959
Attn: Justin Liu	(Customer Number)	
Signature		
Date	January 15, 2004	Charge any additional fees required/credit any overpayment to our Deposit Account Number: 24-0040

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PATENT

IN THE UNITED STATES PATENT OFFICE

Applicant: Aresh M. Menon et al.

Assignee: Xilinx, Inc.

Title: "High Speed Configurable Transceiver Architecture"

Serial No.: 10/090,250

File Date: March 1, 2004

Examiner: Unknown

Art Unit: 2631

Docket No.: X-1050 US

Conf. No.: 4098

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P.O. BOX 1450
Alexandria, VA 22313-1450

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicants bring to the attention of the Examiner the One Hundred Seven (107) references listed in the attached Form PTO-1449. A copy of each is enclosed herein.

These references were cited in related U.S. patent applications. This Information Disclosure Statement is being filed under 37 CFR 1.97(b) prior to the receipt of a first office action.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

Respectfully submitted,

Justin Liu
Attorney for Applicants
Reg. No. 51,959

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Sheet	1	of	7
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Complete if Known

Application / Conf. No.	10/090,250 / 4098
Filing Date	March 01, 2002
First Named Inventor	Suresh M. Menon
Art Unit	2631
Examiner Name	Unknown
Attorney Docket Number	X-1050 US

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
		US- 4,758,985	07-19-88	Carter	
		US- 5,142,625	08-25-92	Nakai	
		US- 4,855,669	08-08-89	Mahoney	
		US- 34,363	08-31-93	Freeman	
		US- 5,072,418	12-10-91	Boutaud et al.	
		US- 5,274,570	12-28-93	Izumi et al.	
		US- 5,550,782	08-27-96	Cliff et al.	
		US- 5,347,181	09-13-94	Ashby et al.	
		US- 5,339,262	08-16-94	Rostoker et al.	
		US- 5,311,114	05-10-94	Sambamurthy et al.	
		US- 5,504,738	04-02-96	Sambamurthy et al.	
		US- 5,552,722	09-03-96	Kean	
		US- 6,467,009	10-15-02	Winegarden et al.	
		US- 5,914,616	06-22-99	Young et al.	
		US- 5,457,410	10-10-95	Ting	
		US- 5,740,404	04-14-98	Baji	
		US- 5,581,745	12-03-96	Muraoka	
		US- 5,742,179	04-21-98	Sasaki	
		US- 5,600,845	02-04-97	Gilson	
		US- 5,574,930	11-12-96	Halverson Jr., et al.	

FOREIGN PATENT DOCUMENTS

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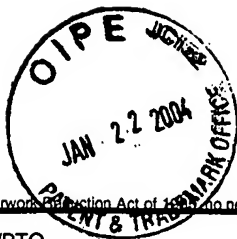
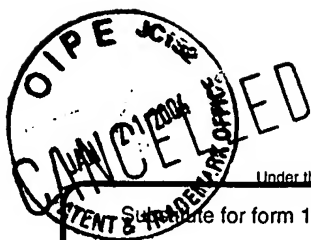
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		Art Unit	2631		
		Examiner Name	Unknown		
Sheet	2	of	7	Attorney Docket Number	X-1050 US

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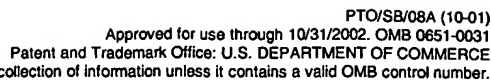
OTHER -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		SAYFE KIAEI et al., "VLSI DESIGN OF DYNAMICALLY RECONFIGURABLE ARRAY PROCESSOR-DRAP," IEEE, February 1989, pp. 2484-2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		VASON P. SRINI, "FIELD PROGRAMMABLE GATE ARRAY (FPGA) IMPLEMENTATION OF DIGITAL SYSTEMS: AN ALTERNATIVE TO ASIC," IEEE, May 1991, pp. 309-314, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		G. MAKI et al., "A RECONFIGURABLE DATA PATH PROCESSOR," IEEE, August 1991, pp. 18-4.1 to 18-4.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		CHRISTIAN ISELI et al., "BEYOND SUPERSCALER USING FPGA's," IEEE, April 1993, pp. 486-490, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		P.C. FRENCH et al., "A SELF-RECONFIGURING PROCESSOR," IEEE, July 1993, pp. 50-59, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		Christian Iseli et al., "SPYDER: A RECONFIGURABLE VLIW PROCESSOR USING FPGA's," IEEE, July 1993, pp. 17-24, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		MICHAEL J. WIRTHLIN et al., "THE NANO PROCESSOR: A LOW RESOURCE RECONFIGURABLE PROCESSOR," IEEE, February 1994, pp. 23-30, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		WILLIAM S. CARTER, "THE FUTURE OF PROGRAMMABLE LOGIC and ITS IMPACT ON DIGITAL SYSTEM DESIGN," April 1994, IEEE, pp. 10-16, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		ANDRE' DEHON, "DPGA-COUPLED MICROPROCESSORS: COMMODITY ICs FOR THE EARLY 21ST CENTURY," IEEE, February 1994, pp. 31 - 39, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		OSAMA T. ALBAHARNA, "AREA & TIME LIMITATIONS OF FPGA-BASED VIRTUAL HARDWARE," IEEE, April 1994, pp. 184 - 189, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	

Examiner Signature	Date Considered
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Sheet	3	of	7
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Application / Conf. No.	10/090,250 / 4098
Filing Date	March 01, 2002
First Named Inventor	Suresh M. Menon
Art Unit	2631
Examiner Name	Unknown
Attorney Docket Number	X-1050 US

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
		US- 5,473,267	12-05-95	Stansfield	
		US- 5,742,180	04-21-98	DeHon et al.	
		US- 5,737,631	04-07-98	Trimberger	
		US- 5,748,979	05-05-98	Trimberger	
		US- 6,578,174	06-10-03	Zizzo	
		US- 6,026,481	02-15-00	New et al.	
		US- 5,705,938	01-06-98	Kean	
		US- 5,500,943	03-19-96	Ho et al.	
		US- 6,483,342	11-19-02	Britton et al.	
		US- 5,809,517	09-15-98	Shimura	
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		US- 5,574,942	11-12-96	Colwell et al.	
		US- 6,604,228	08-05-03	Patel et al.	
		US- 5,933,023	08-03-99	Young	
		US- 10/043,769	01-09-02	Schulz	
		US- 6,389,558	05-14-02	Herrmann et al.	
		US- 5,732,250	03-24-98	Bates et al.	
		US- 5,889,788	03-30-99	Pressly et al.	
		US- 5,874,834	02-23-99	New	
		US- 5,835,405	11-10-98	Tsui et al.	

FOREIGN PATENT DOCUMENTS

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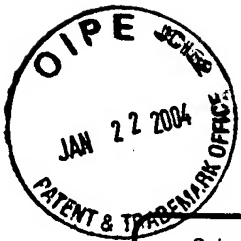
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Attorney Docket Number	X-1050 US

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OTHER -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		<u>XILINX, INC.</u> , "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		<u>XILINX, INC.</u> , "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-109 to 2-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		<u>XILINX, INC.</u> , "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-9 to 2-18; 2-187 to 2-199, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		<u>XILINX, INC.</u> , "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-107 to 2-108, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		<u>CHRISTIAN ISELI et al.</u> , "AC++ COMPILER FOR FPGA CUSTOM EXECUTION UNITS SYNTHESIS," 1995, pp. 173-179, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		<u>INTERNATIONAL BUSINESS MACHINES</u> , "POWERPC 405 EMBEDDED PROCESSOR CORE USER MANUAL" 1996, 5TH Ed., pp. 1-1 TO X-16, International Business Machines, 1580 Rout 52, Bldg. 504, Hopewell Junction, NY 12533-6531.	
		<u>YAMIN LI et al.</u> , "AIZUP-A PIPELINED PROCESSOR DESIGN & IMPLEMENTATION ON XILINX FPGA CHIP," IEEE, September 1996, pp 98-106, 98-106, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		<u>RALPH D. WITTIG et al.</u> , "ONECHIP: AN FPGA PROCESSOR WITH RECONFIGURABLE LOGIC, April 17, 1996, pp 126-135, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		<u>XILINX, INC.</u> , "THE PROGRAMMABLE LOGIC DATA BOOK," January 27, 1999, Ch. 3, pp 3-1 TO 3-50, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	
		<u>WILLIAM B. ANDREW et al.</u> , "A FIELD PROGRAMMABLE SYSTEM CHIP WHICH COMBINES FPGA & ASIC CIRCUITRY," IEEE, May 16, 1999, pp. 183-186, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		<u>XILINX, INC.</u> , "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch. 3 pp 3-1 TO 3-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	

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Sheet	5	of	7
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Filing Date	March 01, 2002
First Named Inventor	Suresh M. Menon
Art Unit	2631
Examiner Name	Unknown
Attorney Docket Number	X-1050 US

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Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
		US- 6,011,407	01-04-00	New	
		US- 6,172,990	01-09-01	Deb et al.	
		US- 10/001,871	11-19-01	Douglass et al.	
		US- 5,760,607	06-02-98	Leeds et al.	
		US- 5,892,961	04-06-99	Trimberger	
		US- 09/991,412	11-16-01	Herron et al.	
		US- 09/991,410	11-16-01	Herron et al.	
		US- 09/968,446	09-28-01	Douglass et al.	
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		US- 6,301,696	10-09-01	Lien et al.	
		US- 6,211,697	04-03-01	Lien et al.	
		US- 6,163,166	12-19-00	Bielby et al.	
		US- 6,272,451	08-07-01	Mason et al.	

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First Named Inventor	Suresh M. Menon
Art Unit	2631
Examiner Name	Unknown
Attorney Docket Number	X-1050 US

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